30V N-Ch Power MOSFET

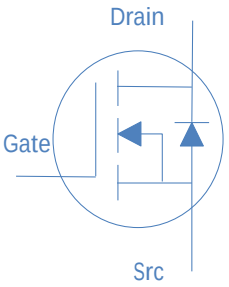
V_{DS}		30	V
$R_{DS(on),typ}$	V_{GS}=10V	15.5	m
$I_{D\ (Sillicon\ Limited)}$		9.5	A

Feature

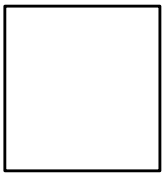
- High Speed Power Switching, Logic Level
- Enhanced Avalanche Ruggedness
- 100% UIS Tested, 100% Rg Tested
- Lead Free, Halogen Free

Application

- Hard Switching and High Speed Circuit
- DC/DC in Telecoms and Inductrial



Part Number	Package	Marking
HTS200N03	SOIC-8	TS200N03



Absolute Maximum Ratings at T_j=25℃ (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	T_A=25℃	9.5	A
		T_A=70℃	7.5	
Drain to Source Voltage	V_{DS}	-	30	V
Gate to Source Voltage	V_{GS}	-	±20	V
Pulsed Drain Current	I_{DM}	-	38	A
Avalanche Energy, Single Pulse	E_{AS}	L=0.1mH, T_C=25℃	3.2	mJ
Power Dissipation	P_D	T_A=25℃	2.5	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to150	℃

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	R_{JA}	50	℃/W
Thermal Resistance Junction-Case	R_{JC}	25	℃/W

Total Gate Charge	Q_g(4.5V)		6.1		nC
		-	1.6		
			10		
		-			

Fig 1. Typical Output Characteristics

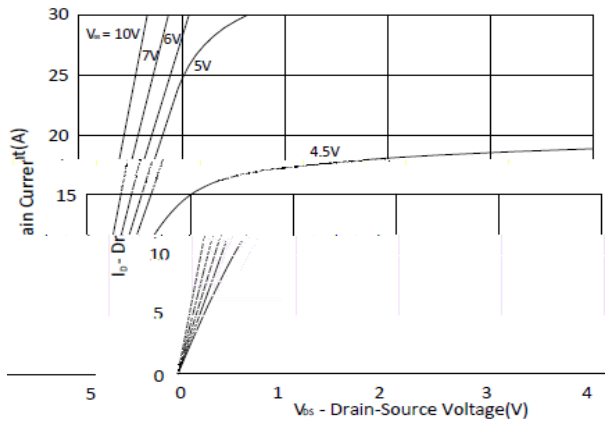


Figure 2. On-Resistance vs. Gate-Source Voltage

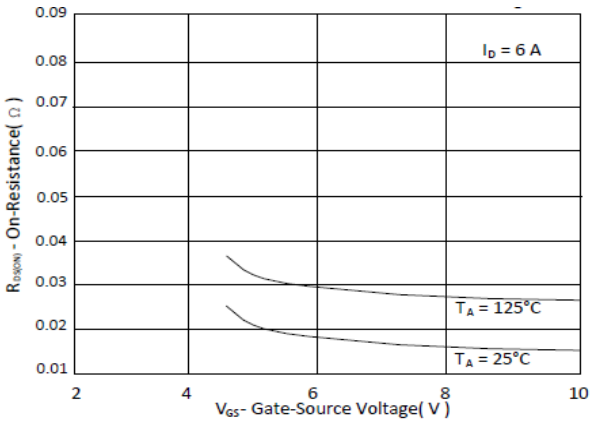


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

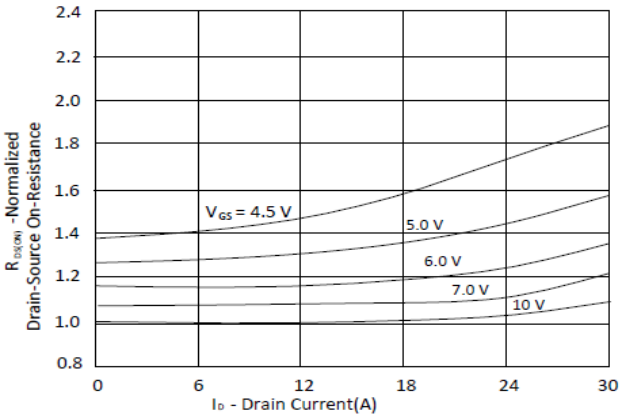


Figure 4. Normalized On-Resistance vs. Junction Temperature

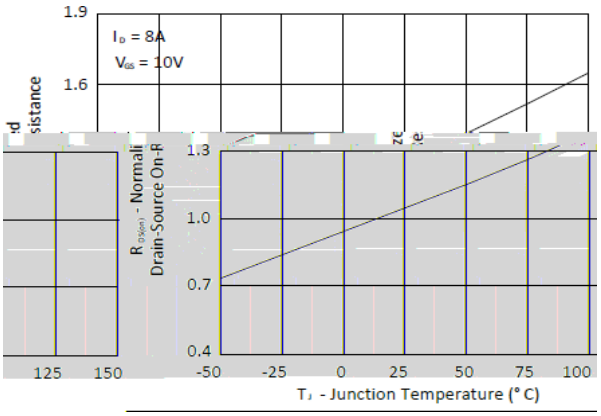


Figure 5. Typical Transfer Characteristics

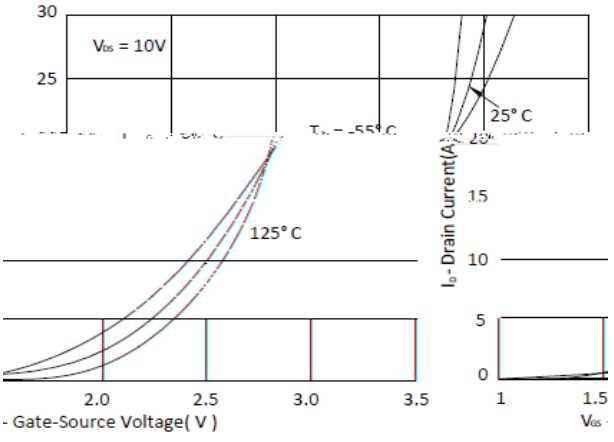


Figure 6. Typical Source-Drain Diode Forward Voltage

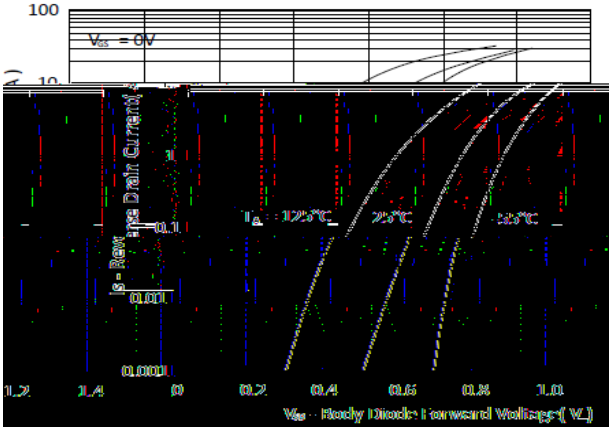


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

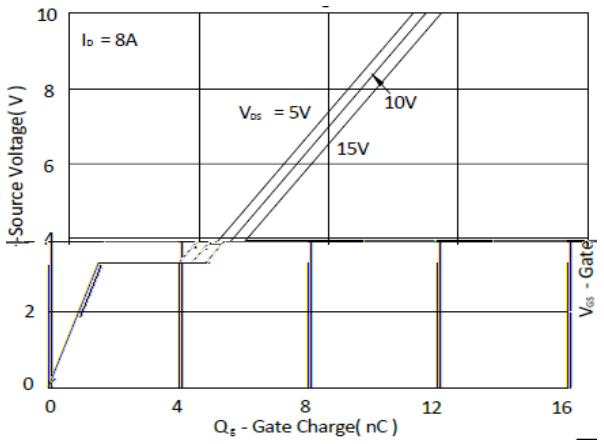


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

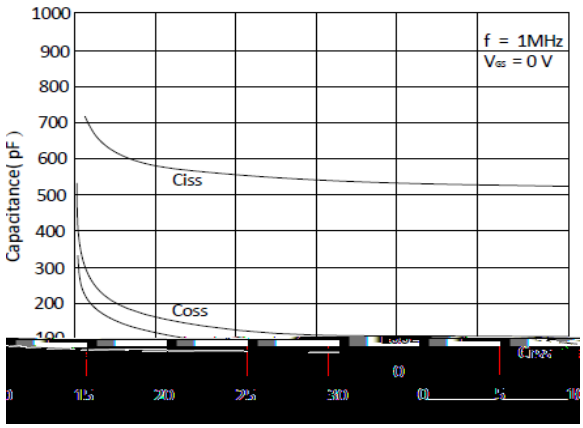


Figure 9. Maximum Safe Operating Area

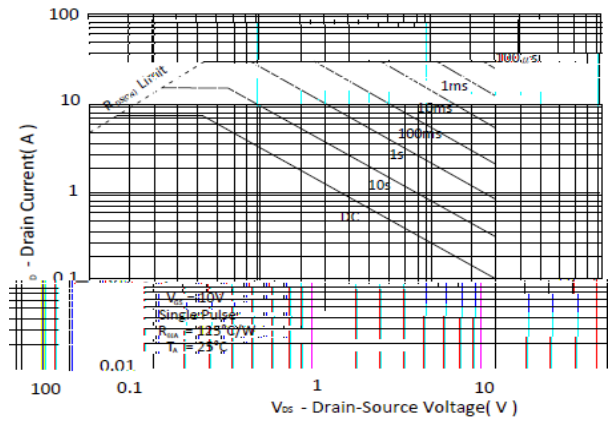


Figure 10. Single Pulse Maximum Power Dissipation

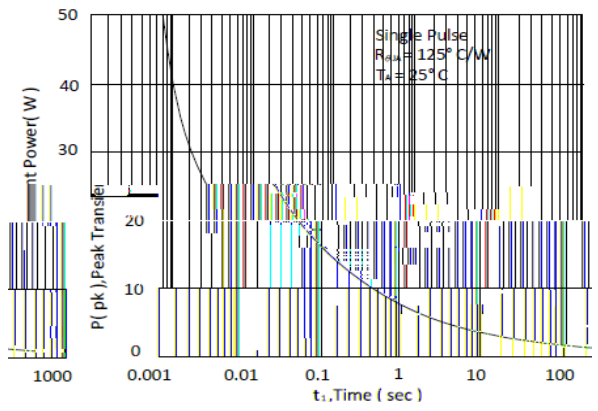
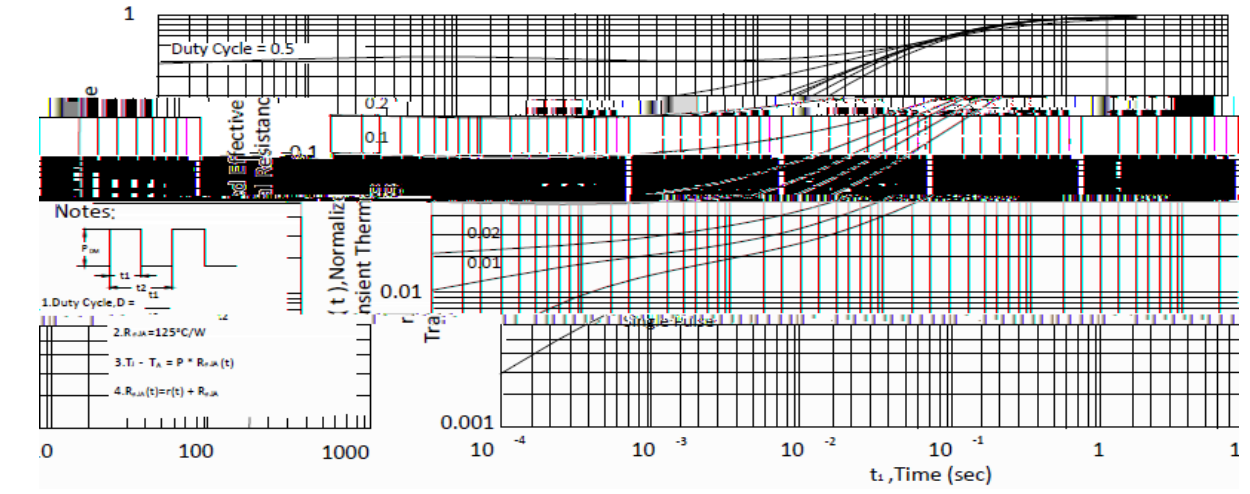
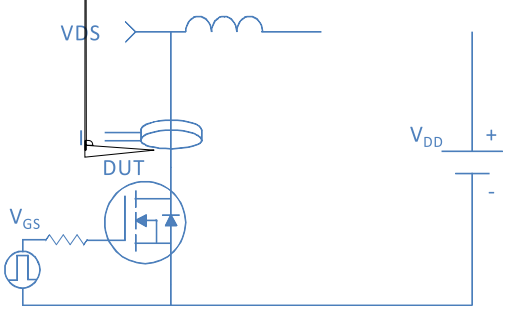


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient



Inductive switching Test	

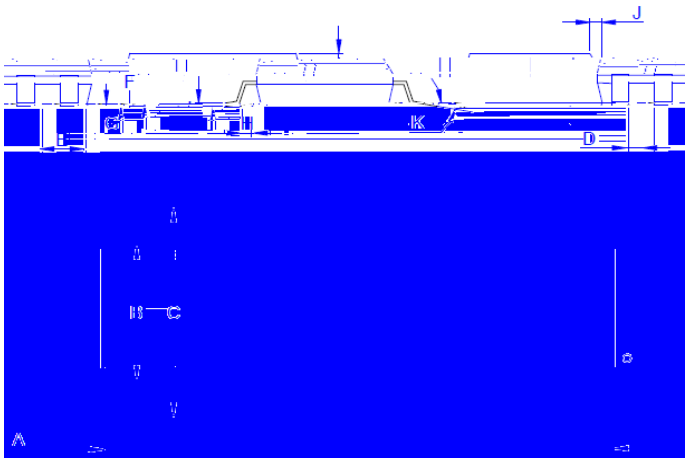
Gate Charge Test	

Uclamped Inductive Switching (UIS) Test	
	

Diode Recovery Test	

Package Outline

SOIC-8, 8 leads



Unit: mm

Dimension	A	B	C	D	E	F	G	H	I	J
Min	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25
Typ.					1.27					
Max	5.10	4.10	6.20	0.51		1.62	0.28	0.88	0.26	0.50